MULTI-SAMPLE READ CIRCUIT HAVING TEST MODE OF OPERATION

ABSTRACT

A data storage device includes non-volatile memory; and a read circuit for performing multi-sample read operations on the memory during a normal mode of operation. The read circuit includes a digital counter having an output that indicates a single bit (e.g., a sign-bit). The read circuit allows an external device (e.g., a memory tester) to supply test clock pulses to an input of the digital counter during a test mode. The test clock pulses can be counted to determine a state of the digital counter.